```
File 348:EUROPEAN PATENTS 1978-2003/Jun W04
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030626,UT=20030619
         (c) 2003 WIPO/Univentio

Set     Items   Description
S1       1031   (SEVEN OR 7)(5N)(BIT OR BITS OR BYTE? ? OR DIGIT? ? OR INT-
             EGER? ? OR FIGURE? ? OR NUMBER? ? OR NUMERAL? ? OR VALUE? ? OR
              CHARACTER? ?)(5N)(DATE OR DATES)
S2        413   (ADD?? OR ADDING OR ADDITION? ? OR SUM? ? OR SUMM??? OR SU-
             MMATION)(5N)(635 OR SIX()HUNDRED(1W)THIRTY()FIVE)
S3         17   (SUBTRACT? OR DEDUCT?)(5N)(635 OR SIX()HUNDRED(1W)THIRTY()-
             FIVE)
S4         39   S2 AND IC=G06F
S5          2   S3 AND IC=G06F
S6         10   S1 AND S2:S3
S7          1   S6 AND IC=G06F
S8         40   S4:S5 NOT S7
```

8/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01446722
Denormalization circuit
Denormalisationsschaltung
Circuit de denormalisation
PATENT ASSIGNEE:
Nokia Corporation, (3988870), Keilalahdentie 4, 02150 Espoo, (FI),
(Applicant designated States: all)
INVENTOR:
McGovern, Brian, 50 Rivermead Road, Camberley, Surrey GU15 2SE, (GB)
Gabzdyl, Rebecca, Badgers, Coach House Close, Frimley, Surrey GU16 5TR, (GB)
Keir, Stefan, 50 Rivermead Road, Camberly, Surrey 16 5TR, (GB)
LEGAL REPRESENTATIVE:
Johnson, Ian Michael (92872), Nokia IPR Department, Nokia House, Summit Avenue, Farnborough, Hants GU14 0NG, (GB)
PATENT (CC, No, Kind, Date): EP 1237070 A2 020904 (Basic)
APPLICATION (CC, No, Date): EP 2002012689 980313;
PRIORITY (CC, No, Date): GB 9705364 970314
DESIGNATED STATES: DE; FR; GB; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 864968 (EP 98301929)
INTERNATIONAL PATENT CLASS: **G06F-007/50 ; G06F-007/48**

ABSTRACT EP 1237070 A2
A data processing circuit is disclosed which is configured to minimise the number of operations required by processing logic so as to reduce overall battery consumption. Arithmetic logic units (605, 606) are configurable to perform operations including the generation of exponent values. A separate comparing unit (618) is configurable to compare exponent values and to store one of said pair of exponent values dependent upon the result of said comparison. This comparison value then remains available for subsequent operations performed by associate circuitry, including arithmetic logic units (605, 606) and a normalisation circuit (619). A normalisation circuit determines the extent to which associate mantissa require shifting operations to be performed in order to normalise a block of floating point values.
ABSTRACT WORD COUNT: 121
NOTE:
Figure number on first page: 6

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 020904 A2 Published application without search report
Withdrawal: 030129 A2 Date of withdrawal of application: 20021004
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200236	698
SPEC A	(English)	200236	4836
Total word count - document A			5534
Total word count - document B			0
Total word count - documents A + B			5534

INTERNATIONAL PATENT CLASS: **G06F-007/50** ...

... **G06F-007/48**

...SPECIFICATION order input word multiplexer 1152 is further capable receiving as an alternate input the output exponent from the normalising unit 619, represented as a bus **635** . The output of the **additional** multiplexer 1154 is supplied as an input to a compare and select register 1157, its contents typically represent the highest of a sequence of compared...

8/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01203266
Methods and apparatus for storage and retrieval of name space information in a distributed computing system
Verfahren und Vorrichtung zum Speichern und Wiederauffinden von Informationen uber den Namenraum in einem verteilten Rechnersystem
Methodes et dispositif pour le stockage et le recouvrement d'informations concernant l'espace des noms dans un systeme informatique distribue
PATENT ASSIGNEE:
AT&T IPM Corp., (1907680), 2333 Ponce de Leon Boulevard, Coral Gables, Florida 33134, (US), (Proprietor designated states: all)
INVENTOR:
Winterbottom, Philip Steven, 800 Johnston Drive, Watchung, Somerset, NJ 07060, (US)
LEGAL REPRESENTATIVE:
Buckley, Christopher Simon Thirsk et al (28912), Lucent Technologies (UK) Ltd, 5 Mornington Road, Woodford Green, Essex IG8 0TU, (GB)
PATENT (CC, No, Kind, Date): EP 1046990 A2 001025 (Basic)
EP 1046990 A3 001102
EP 1046990 B1 030108
APPLICATION (CC, No, Date): EP 2000117414 960410;
PRIORITY (CC, No, Date): US 424137 950417
DESIGNATED STATES: DE; FR; GB
RELATED PARENT NUMBER(S) - PN (AN):
EP 738970 (EP 96302502)
INTERNATIONAL PATENT CLASS: **G06F-009/46 ; G06F-017/30**
CITED PATENTS (EP B): EP 466486 A
CITED REFERENCES (EP B):
RADIA S: "Naming policies in the Spring system" PROCEEDINGS. FIRST INTERNATIONAL WORKSHOP ON SERVICES IN DISTRIBUTED AND NETWORKED ENVIRONMENTS (CAT. NO.94TH0627-0), PROCEEDINGS OF IEEE WORKSHOP ON SERVICES FOR DISTRIBUTED AND NETWORKED ENVIRONMENTS, PRAGUE, CZECH REPUBLIC, 27-28 JUNE 1994, pages 164-171, XP000577565 ISBN 0-8186-5835-5, 1994, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC. PRESS, USA
OUSTERHOUT J K ET AL: "THE SPRITE NETWORK OPERATING SYSTEM" COMPUTER, vol. 21, no. 2, 1 February 1988 (1988-02-01), pages 23-36, XP000111082
WELCH B: "A comparison of three distributed file system architectures: vnode, Sprite, and Plan 9" COMPUTING SYSTEMS, SPRING 1994, USA, vol. 7, no. 2, pages 175-199, XP000577569 ISSN 0895-6340
Inside Microsoft Windows NT, David A. Solomon, Microsoft Press, 2. Ed., publ. 1998, p. 409-413;

ABSTRACT EP 1046990 A3
A distributed computing environment is disclosed which allows a user at one location to access resources at other locations. Each resource in the distributed computing environment is represented as a hierarchical file system. A user or process has a name space comprised of at least one hierarchical file system provided by a connected resource. The distributed computing environment allows a first processor to invoke execution of a processing task by a remote processor. The first processor transmits a representation of its current name space to the remote processor. The remote processor will execute the processing task on a name space modified in accordance with the name space representation received from the first processor. The transmitted representation of the name space associated with the first processor includes at least one dynamic name space modification command, such as those executed by a user after logging into the distributed computing system. A plurality of data structures are provided for storing path information which allows the pathname of a given channel, which represents a file, to be determined. The stored path information allows the hierarchical file tree of a connected file system to be generated.
ABSTRACT WORD COUNT: 192
NOTE:
Figure number on first page: NONE

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 001025 A2 Published application without search report
 Examination: 001025 A2 Date of request for examination: 20000824
 Change: 001102 A2 International Patent Classification changed:
  20000913
 Search Report: 001102 A3 Separate publication of the search report
 Change: 010117 A2 Inventor information changed: 20001128
 Examination: 011114 A2 Date of dispatch of the first examination
  report: 20011002
 Grant: 030108 B1 Granted patent
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
 CLAIMS A (English) 200043 549
 CLAIMS B (English) 200302 555
 CLAIMS B (German) 200302 468
 CLAIMS B (French) 200302 620
 SPEC A (English) 200043 21025
 SPEC B (English) 200302 20585
Total word count - document A 21577
Total word count - document B 22228
Total word count - documents A + B 43805
INTERNATIONAL PATENT CLASS: **G06F-009/46** ...

... **G06F-017/30**

...SPECIFICATION is preferably incremented during step 1340 to the channel corresponding to the next element in the linked list 880 which forms the union directory. In **addition** , the value of the pointer **635** in the channel which the union directory has been mounted upon is preferably updated during step 1342 to indicate the current directory in the union ...

...SPECIFICATION is preferably incremented during step 1340 to the channel corresponding to the next element in the linked list 880 which forms the union directory. In **addition** , the value of the pointer **635** in the channel which the union directory has been mounted upon is preferably updated during step 1342 to indicate the current directory in the union ...

8/5,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01081178
Methods and apparatus for linking a program for remote execution
Verfahren und Gerat zur Verknupfung eines Programmes zur Fernausfuhrung
Methodes et appareil pour lier un logiciel pour execution a distance
PATENT ASSIGNEE:
 Sun Microsystems, Inc., (2616583), 901 San Antonio Road, M/S PAL01-521, Palo Alto, California 94304, (US), (Applicant designated States: all)
INVENTOR:
 Madany, Peter W., 1125 Geddy Way, Fremont, California 94539, (US)
 Tuck, Richard, 343 Hill Street, San Francisco, California 94114, (US)
 Fresko, Nedim, 1366 5th Avenue, Apartment No. 2, San Francisco, California 94122-2667, (US)
LEGAL REPRESENTATIVE:
 Beresford, Keith Denis Lewis et al (28275), Beresford & Co., 2-5 Warwick Court, High Holborn, London WC1R 5DH, (GB)
PATENT (CC, No, Kind, Date): EP 950950 A2 991020 (Basic)
APPLICATION (CC, No, Date): EP 99400685 990319;
PRIORITY (CC, No, Date): US 44904 980320
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-009/445**

ABSTRACT EP 950950 A2

A linkage editor executing at a server receives instructions for packaging software components that are required for program execution at a client. The linkage editor generates an output file by iteratively analyzing the program for references to other software components and extracting those components from their parent classes. The linkage editor sends the completed output file to an interface task, which transmits it to the client.

ABSTRACT WORD COUNT: 67

NOTE:

Figure number on first page: 6

LEGAL STATUS (Type, Pub Date, Kind, Text):

Assignee:	020508	A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616582) 901 San Antonio Road, M/S UPAL 01-521 Palo Alto, California 94303 US
Application:	991020	A2	Published application without search report
Change:	030528	A2	Legal representative(s) changed 20030409
Assignee:	030528	A2	Transfer of rights to new applicant: Sun Microsystems, Inc. (2616592) 4150 Network Circle Santa Clara, California 95054 US

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9942	831
SPEC A	(English)	9942	4492
Total word count - document A			5323
Total word count - document B			0
Total word count - documents A + B			5323

INTERNATIONAL PATENT CLASS: **G06F-009/445**

...SPECIFICATION file, along with the ancillary inforrnation associated with their classes (steps 625-630). Linkage editor 487 will discover that component C1 references component C1A (step **635**), and will **add** it to the component list (step 645). The process repeats one more time, during which component C1A is extracted from its respective class (along with...

8/5,K/5 (Item 5 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

01037283

DATA TRANSFER TO A NON-VOLATILE STORAGE MEDIUM

DATENUBERTRAGUNG AUF EINEM NICHTFLUCHTIGEN SPEICHERMEDIUM

TRANSFERT DE DONNEES VERS UNE MEMOIRE REMANENTE

PATENT ASSIGNEE:

Phoenix Technologies Limited, (2631810), 411 East Plumeria Drive, San Jose, CA 95134, (US), (Proprietor designated states: all)

INVENTOR:

LEWIS, Timothy, 33775 Shallow Court, Fremont, CA 94555, (US)

LEGAL REPRESENTATIVE:

Naismith, Robert Stewart et al (57811), CRUIKSHANK & FAIRWEATHER 19 Royal Exchange Square, Glasgow, G1 3AE Scotland, (GB)

PATENT (CC, No, Kind, Date): EP 1015976 A1 000705 (Basic)
EP 1015976 B1 020306
WO 9914673 990325

APPLICATION (CC, No, Date): EP 98948205 980916; WO 98US19128 980916

PRIORITY (CC, No, Date): US 931330 970916

DESIGNATED STATES: DE; GB

INTERNATIONAL PATENT CLASS: **G06F-011/14**

CITED PATENTS (EP B): EP 636978 A; EP 658843 A

CITED PATENTS (WO A): XP 534434 ; XP 587466

CITED REFERENCES (EP B):

"Hibernating and Resuming a Compressed Memory Image" IBM TECHNICAL DISCLOSURE BULLETIN., vol. 38, no. 8, August 1995, page 73 XP000534434

NEW YORK US
"Automatic Data Compression Control for Hibernation" IBM TECHNICAL DISCLOSURE BULLETIN., vol. 39, no. 4, April 1996, pages 185-186, XP000587466 NEW YORK US;
CITED REFERENCES (WO A):
"Hibernating and Resuming a Compressed Memory Image" IBM TECHNICAL DISCLOSURE BULLETIN., vol. 38, no. 8, August 1995, page 73 XP000534434 NEW YORK US
"Automatic Data Compression Control for Hibernation" IBM TECHNICAL DISCLOSURE BULLETIN., vol. 39, no. 4, April 1996, pages 185-186, XP000587466 NEW YORK US;
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	000705 A1	Published application with search report
Application:	990602 A1	International application (Art. 158(1))
Oppn None:	030226 B1	No opposition filed: 20021209
Examination:	001025 A1	Date of dispatch of the first examination report: 20000912
Examination:	000705 A1	Date of request for examination: 20000331
Grant:	020306 B1	Granted patent

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200210	1298
CLAIMS B	(German)	200210	1257
CLAIMS B	(French)	200210	1586
SPEC B	(English)	200210	8169
Total word count - document A			0
Total word count - document B			12310
Total word count - documents A + B			12310

INTERNATIONAL PATENT CLASS: **G06F-011/14**

...SPECIFICATION transfer size must be performed by pmDiskWrite, so Sectors is set equal 630 to Size/SectorSize before a write to disk is performed by pmDiskWrite **635** . Then 640, (Sectors*SectorSize) is **subtracted** from Size so that Size represents the quantity of data which remains in the buffer 120 to be written to disk, and Location is incremented...

8/5,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00977316
Method and apparatus to expand an on-chip fifo into local memory
Verfahren und Vorrichtung zum Erweitern eines on-chip Fifos in einem lokalen Speicher
Procede et dispositif d'extension d'un fifo sur-puce dans une memoire locale
PATENT ASSIGNEE:
Compaq Computer Corporation, (687792), 20555 S.H. 249, Houston Texas 77070, (US), (Applicant designated States: all)
INVENTOR:
Ben-Michael, Simoni, 13/3 Mitzpe Street, Givat Zeev 90917, (IL)
Ben-Shahar, Yifat, Meron Street 24/18, Mevaseret Zion 90805, (IL)
Ben-Nun, Michael, Derech Hahoresh 34/2, Ramot Ayalon, Jerusalem, (IL)
LEGAL REPRESENTATIVE:
Charig, Raymond Julian et al (79692), Eric Potter Clarkson, Park View House, 58 The Ropewalk, Nottingham NG1 5DD, (GB)
PATENT (CC, No, Kind, Date): EP 886454 A2 981223 (Basic)
EP 886454 A3 000920
APPLICATION (CC, No, Date): EP 98304594 980610;
PRIORITY (CC, No, Date): US 879359 970620
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04Q-011/04; **G06F-005/06** ; H04L-012/56

ABSTRACT EP 886454 A2

A relatively small FIFO queue is located on a semiconductor chip receiving and transmitting data in a computer system, typically a computer network. The FIFO queue has additional storage capability in the form of an expansion into the local memory of the computer system. The front and back ends of the FIFO, which are involved in receiving and transmitting data, are implemented on the chip. The FIFO expands into the space provided in the local memory only when the on-chip portion of the FIFO is full. The middle portion of the FIFO resides in expansion in the local memory. The local memory is accessed only in bursts of multiple credits, both for read transactions and for write transactions.

ABSTRACT WORD COUNT: 119

NOTE:

Figure number on first page: 7

LEGAL STATUS (Type, Pub Date, Kind, Text):

Assignee:	000531	A2	Transfer of rights to new applicant: Compaq Computer Corporation (687792) 20555 S.H. 249 Houston Texas 77070 US
Application:	981223	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	000920	A3	Separate publication of the search report
Change:	000920	A2	International Patent Classification changed: 20000801
Examination:	010502	A2	Date of request for examination: 20010302

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9852	698
SPEC A	(English)	9852	5304
Total word count - document A			6002
Total word count - document B			0
Total word count - documents A + B			6002

...INTERNATIONAL PATENT CLASS: **G06F-005/06**

...SPECIFICATION are more than 16K credits in the local memory FIFO expansion 720, the delayed FIFO 600 gets full priority over the activate FIFO 610.

In **addition** , the programmable bit **635** in the Command and Status Register 630 (CSR) which, when set, will force the arbiter 620 to return credits from the delayed FIFO 600 only...

8/5,K/7 (Item 7 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00966551

Data processing circuit

Datenverarbeitungsschaltung

Circuit a traitement de donnees

PATENT ASSIGNEE:

NOKIA MOBILE PHONES LTD., (997966), Keilalahdentie 4, 02150 Espoo, (FI), (Applicant designated States: all)

INVENTOR:

Gabzdyl, Rebecca, Badgers, Coach House Close, Frimley, Surrey GU16 5TR, (GB)

McGovern, Brian Patrick, 50 Rivermead Road, Camberley, Surrey GU15 2SE, (GB)

LEGAL REPRESENTATIVE:

Haws, Helen Louise et al (72992), Nokia IPR Department Nokia (UK) Limited Summit Avenue Southwood, Farnborough Hampshire GU14 0NZ, (GB)

PATENT (CC, No, Kind, Date): EP 877315 A2 981111 (Basic)
EP 877315 A3 020213

APPLICATION (CC, No, Date): EP 98301931 980313;

PRIORITY (CC, No, Date): GB 9705295 970314

DESIGNATED STATES: DE; FR; GB; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-009/302**

ABSTRACT EP 877315 A2
A data processing circuit includes a first set of processing elements and a second set of processing elements. A clock provides common clocking signals to the processing elements, however, the first set of elements are clocked by rising edges of the clocking signals and the second set of elements are clocked by falling edges of the clocking signals.
ABSTRACT WORD COUNT: 59
NOTE:
Figure number on first page: 6

LEGAL STATUS (Type, Pub Date, Kind, Text):
Search Report: 020213 A3 Separate publication of the search report
Application: 981111 A2 Published application (A1with Search Report ;A2without Search Report)
Assignee: 020313 A2 Transfer of rights to new applicant: Nokia Corporation (3988870) Keilalahdentie 4 02150 Espoo FI
Examination: 021016 A2 Date of request for examination: 20020813
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9846	389
SPEC A	(English)	9846	4606
Total word count - document A			4995
Total word count - document B			0
Total word count - documents A + B			4995

INTERNATIONAL PATENT CLASS: **G06F-009/302**

...SPECIFICATION order input word multiplexer 1152 is further capable receiving as an alternate input the output exponent from the normalising unit 619, represented as a bus **635** . The output of the **additional** multiplexer 1154 is supplied as an input to a compare and select register 1157, its contents typically represent the highest of a sequence of compared...

8/5,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00884212
Apparatus and method for the availability and recovery of files using copy storage pools
Vorrichtung und Verfahren fur die Verfugbarkeit und Wiedergewinnung von Dateien unter Verwendung von Sammlungen von Kopierspeicher
Dispositif et methode de disposibilite et recuperation de fichiers utilisant des ensembles de memoires de copie
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (Proprietor designated states: all)
INVENTOR:
Cannon, David Maxwell, 8603 E. 24th Street, Tucson, Arizona 85710, (US)
Kaczmarski, Michael Allen, 1481 N. Placita Ombria, Tucson, Arizona 85715, (US)
Warren, Donald Paul, Jr., 1067 W. Pennsylvania, Tucson, Arizona 85714, (US)
LEGAL REPRESENTATIVE:
Zerbi, Guido Maria (77893), Intellectual Property Department, IBM United Kingdom Ltd., Hursley Park, Winchester, Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 809184 A1 971126 (Basic)
EP 809184 B1 020731
APPLICATION (CC, No, Date): EP 97303323 970515;
PRIORITY (CC, No, Date): US 652042 960523

DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-011/14**
CITED PATENTS (EP B): EP 359471 A; EP 593062 A

ABSTRACT EP 809184 A1
A data processing system using a client-server configuration provides a method and apparatus for generating and managing multiple copies of client data files. A server coupled to a plurality of client systems organizes sets of storage volumes into storage pools. Primary copies of the client data files are stored in primary storage pools while additional back-up copies of the client data files are copied to secondary storage pools, called copy storage pools. A server database maintains directory information about the original client data file and reference information about the location of the multiple file copies within the server. A storage manager provides a control centre within the server, directing and coordinating the transfer of files between the various storage pools, and updating the server database with directory and reference location information.
ABSTRACT WORD COUNT: 132
NOTE:
Figure number on first page: NONE

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	001206	A1	Date of dispatch of the first examination report: 20001020
Application:	971126	A1	Published application (A1with Search Report ;A2without Search Report)
Grant:	020731	B1	Granted patent
Change:	010808	A1	Title of invention (German) changed: 20010618
Change:	010808	A1	Title of invention (English) changed: 20010618
Change:	010808	A1	Title of invention (French) changed: 20010618
Examination:	980422	A1	Date of filing of request for examination: 980224

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199711W3	1738
CLAIMS B	(English)	200231	1980
CLAIMS B	(German)	200231	1762
CLAIMS B	(French)	200231	2495
SPEC A	(English)	199711W3	7404
SPEC B	(English)	200231	7142
Total word count - document A			9143
Total word count - document B			13379
Total word count - documents A + B			22522

INTERNATIONAL PATENT CLASS: **G06F-011/14**

...SPECIFICATION which copy storage volume 51-54 fits the "best" label, such as storage volume location, storage volume availability, and mount status and time. A step **635** **adds** the selected copy storage volume 51-54 to a list of best storage volumes, provided the volume is not previously included in the list. A...

...SPECIFICATION which copy storage volume 51-54 fits the "best" label, such as storage volume location, storage volume availability, and mount status and time. A step **635** **adds** the selected copy storage volume 51-54 to a list of best storage volumes, provided the volume is not previously included in the

8/5,K/12 (Item 12 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00793329
Methods and apparatus for storage and retrieval of name space information in a distributed computing system

Verfahren und Vorrichtung zum Speichern und Wiederauffinden von Informationen uber den Namenraum in einem verteilten Rechnersystem
Methodes et dispositif pour le stockage et le recouvrement d'informations concernant l'espace des noms dans un systeme informatique distribue

PATENT ASSIGNEE:
AT&T IPM Corp., (1907680), 2333 Ponce de Leon Boulevard, Coral Gables, Florida 33134, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Winterbottom, Philip Steven, 591 Mountain Avenue, Apt. No. 8, Gillette, New Jersey 07933, (US)
LEGAL REPRESENTATIVE:
Johnston, Kenneth Graham (32381), Lucent Technologies (UK) Ltd, 5 Mornington Road, Woodford Green Essex, IG8 OTU, (GB)
PATENT (CC, No, Kind, Date): EP 738970 A1 961023 (Basic)
APPLICATION (CC, No, Date): EP 96302502 960410;
PRIORITY (CC, No, Date): US 424137 950417
DESIGNATED STATES: DE; FR; GB
RELATED DIVISIONAL NUMBER(S) - PN (AN):
(EP 117414)
INTERNATIONAL PATENT CLASS: **G06F-009/46 ; G06F-017/30**

ABSTRACT EP 738970 A1
A distributed computing environment is disclosed which allows a user at one location to access resources at other locations. Each resource in the distributed computing environment is represented as a hierarchical file system. A user or process has a name space comprised of at least one hierarchical file system provided by a connected resource. The distributed computing environment allows a first processor to invoke execution of a processing task by a remote processor. The first processor transmits a representation of its current name space to the remote processor. The remote processor will execute the processing task on a name space modified in accordance with the name space representation received from the first processor. The transmitted representation of the name space associated with the first processor includes at least one dynamic name space modification command, such as those executed by a user after logging into the distributed computing system. A plurality of data structures are provided for storing path information which allows the pathname of a given channel, which represents a file, to be determined. The stored path information allows the hierarchical file tree of a connected file system to be generated.
(see image in original document)
ABSTRACT WORD COUNT: 226

LEGAL STATUS (Type, Pub Date, Kind, Text):

Change:	001004 A1	Application number of divisional application (Article 76) changed: 20000817
Examination:	20000412 A1	Date of dispatch of the first examination report: 20000228
Application:	961023 A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	970611 A1	Date of filing of request for examination: 970410

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	1265
SPEC A	(English)	EPAB96	21026
Total word count - document A			22291
Total word count - document B			0
Total word count - documents A + B			22291

INTERNATIONAL PATENT CLASS: **G06F-009/46 ...**
... G06F-017/30

...SPECIFICATION is preferably incremented during step 1340 to the channel corresponding to the next element in the linked list 880 which forms the union directory. In **addition** , the value of the pointer **635** in the channel which the union directory has been mounted upon is preferably

updated during step 1342 to indicate the current directory in the union...

8/5,K/13 (Item 13 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00793218

Multiplier
Multiplizierer
Multiplieur

PATENT ASSIGNEE:
THOMSON multimedia, (1090172), 46 quai A. Le Gallo, 92648 Boulogne Cedex, (FR), (applicant designated states: DE;ES;FR;GB;IT)

INVENTOR:
Chan Yan Fong, Joseph, 61, Domaine de 1'Ile, 67400 Illkirch, (FR)

LEGAL REPRESENTATIVE:
Hartnack, Wolfgang, Dipl.-Ing. et al (78102), Deutsche Thomson-Brandt GmbH Licensing & Intellectual Property, Karl-Wiechert-Alee 74, 30625 Hannover, (DE)

PATENT (CC, No, Kind, Date): EP 738958 A2 961023 (Basic)
EP 738958 A3 970115
EP 738958 B1 990707

APPLICATION (CC, No, Date): EP 96109443 921012;

PRIORITY (CC, No, Date): EP 91402797 911021

DESIGNATED STATES: DE; ES; FR; GB; IT

RELATED PARENT NUMBER(S) - PN (AN):
EP 610259 (EP 929212223)

INTERNATIONAL PATENT CLASS: **G06F-007/52 ; G06F-007/50**

ABSTRACT EP 738958 A2

E.g. for video applications fast multipliers with high resolution are required. But a higher resolution results in more partial products to be calculated internally. The Booth-McSorley algorithm can be used in order to reduce the required number of such partial products. This algorithm can be combined with a diagonal propagation of the carry from one partial product to the other, allowing all the sums on a line to be calculated simultaneously. But the reachable multiplication time is not short enough.

The inventive multiplier in nearly full CMOS design has been constructed with a 1.2(mu) BICMOS technology, having a multiplication time of 9ns with a supply voltage of 5 volts. Minimum multiplication time has been achieved by a combination of the following techniques:
- use of the Booth-McSorley algorithm in order to reduce the number of partial products;
- diagonal propagation of the carry from one partial product to the other allowing all the sums on one line to be done simultaneously;
- use of the carry select approach in the final 14 bits adder and in the first two adders in the intermediate rows;
- use of fast one-bit full adders with complementary pass transistor logic. (see image in original document)

ABSTRACT WORD COUNT: 232

LEGAL STATUS (Type, Pub Date, Kind, Text):

Oppn None:	000628 B1	No opposition filed: 20000408
Application:	961023 A2	Published application (A1with Search Report ;A2without Search Report)
Change:	970102 A2	Obligatory supplementary classification (change)
Search Report:	970115 A3	Separate publication of the European or International search report
Examination:	970806 A2	Date of filing of request for examination: 970605
*Assignee:	980325 A2	Applicant (transfer of rights) (change): THOMSON multimedia (1090172) 46, Quai A. Le Gallo 92648 Boulogne Cedex (FR) (applicant

designated states: DE;ES;FR;GB;IT)
*Assignee: 980325 A2 Previous applicant in case of transfer of rights (change): THOMSON multimedia (1090174) 9, place des Vosges La Defense 5 92400 Courbevoie (FR) (applicant designated states: DE;ES;FR;GB;IT)
Examination: 981104 A2 Date of despatch of first examination report: 980916
Grant: 990707 B1 Granted patent
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9927	1325
CLAIMS B	(German)	9927	1226
CLAIMS B	(French)	9927	1366
SPEC B	(English)	9927	4354
Total word count - document A			0
Total word count - document B			8271
Total word count - documents A + B			8271

INTERNATIONAL PATENT CLASS: **G06F-007/52** ...

... **G06F-007/50**

...SPECIFICATION contains 4-bit full adders 611, 621, 616 and 626, 3-bit full adders 631 and 636 with normal carry input, a 3-bit full **adder 635** with complementary carry input and 2:1 multiplexers 612 - 615, 622 - 625, 632 - 634, 617, 627 and 637. The input signals a0, b0, a1, b1, a2 and b3 of **adder 635** stem from the **sum** and carry outputs of the basic building blocks FA in sixth row 418 which follow directly the respective adding circuit. The input signals of adders...

...represent output signals S20 - S23, S16 - S19 and S13 - S15 of the upper bits of the 24-bit result of the multiplication. Carry input of **adder 635** is connected to the one clock delayed complementation command signal C' generated in Booth encoder circuit 408 which has been latched in static latch 624. This latch is controlled by clock signals H and HB. The carry output of **adder 635** is connected to an inverter 641 and to the switching input of multiplexer 637. The output of inverter 641 is connected to the switching inputs...according to Fig. 12 the 3-bit adder has a complementary carry input CI.

E.g. the input signals a0 - a2 and b0 - b2 for **adder 635** are fed to respective connected parallel 1-bit adders. Input signals a0 and b0 and carry input CI are fed to adder 81 which outputs...

...CLAIMS pipeline row (413, 416, 419);
- a last row (410) with a carry select adder circuit which is constructed from one 4- and/or 3-bit **adder** circuit (**635**) and/or pairs of said 4- and/or 3-bit adder circuits (611,616; 621,626; 631,636), which contain said 1-bit adders (+).
2...

8/5,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00719969
Space vector data path
Raumzeigersdatenpfad
Chemin de donnees de vecteur d'espace
PATENT ASSIGNEE:
Conexant Systems, Inc., (2732580), 4311 Jamboree Road, Newport Beach, California 92660-3095, (US), (Proprietor designated states: all)
INVENTOR:
Bindloss, Keith M., 3861 Beaver Street, Irvine, California 92714, (US)
Garey, Kenneth E., 17531 Friends Court, Irvine, California 92714, (US)

Watson, George A., 2952 Treeview Place, Fullerton, California 92635, (US)
Earle, John, 15512-P Williams Street, Tustin, California 92680, (US)
LEGAL REPRESENTATIVE:
Wagner, Karl H., Dipl.-Ing. et al (12561), WAGNER & GEYER Patentanwalte Gewurzmuhlstrasse 5, 80538 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 681236 A1 951108 (Basic)
EP 681236 B1 001122
APPLICATION (CC, No, Date): EP 95106843 950505;
PRIORITY (CC, No, Date): US 238558 940505
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-009/302**
CITED PATENTS (EP B): EP 395348 A; EP 464601 A; GB 2136172 A; US 4161784 A

ABSTRACT EP 681236 A1
A space vector path for integrating SIMD scheme into a general-purpose programmable processor is disclosed. The programmable processor comprises mode means coupled to an instruction means (130, 140) for specifying for each instruction whether an operand is processed in one of vector and scalar modes, processing unit (110) coupled to the mode means for receiving the operand and, responsive to an instruction as specified by the mode means, for processing the operand in one of the vector and scalar modes, wherein the vector mode indicating to the processing unit (110) that there are a plurality of elements within the operand and the scalar mode indicating to the processing unit (110) that there is one element within the operand. (see image in original document)
ABSTRACT WORD COUNT: 125
NOTE:
Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):

Assignee:	000712	A1	Transfer of rights to new applicant: Conexant Systems, Inc. (2732580) 4311 Jamboree Road Newport Beach, California 92660-3095 US
Application:	951108	A1	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	011114	B1	No opposition filed: 20010823
Grant:	001122	B1	Granted patent
Examination:	960320	A1	Date of filing of request for examination: 960119
Examination:	990506	A1	Date of despatch of first examination report: 990318

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200047	772
CLAIMS B	(German)	200047	746
CLAIMS B	(French)	200047	804
SPEC B	(English)	200047	10744
Total word count - document A			0
Total word count - document B			13066
Total word count - documents A + B			13066

INTERNATIONAL PATENT CLASS: **G06F-009/302**

8/5,K/15 (Item 15 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00625760
1-BIT ADDER
EINZELBITADDIERER
ADDITIONNEUR 1 BIT
PATENT ASSIGNEE:
THOMSON multimedia, (1090174), 9, place des Vosges La Defense 5, 92400 Courbevoie, (FR), (applicant designated states: DE;ES;FR;GB;IT)
INVENTOR:
CHAN YAN FONG, Joseph, 61, domaine de l'Ile, F-67400 Illkirch, (FR)

LEGAL REPRESENTATIVE:
  Hartnack, Wolfgang, Dipl.-Ing. et al (78102), Deutsche Thomson-Brandt GmbH Licensing & Intellectual Property, Gottinger Chaussee 76, 30453 Hannover, (DE)
PATENT (CC, No, Kind, Date): EP 610259 A1 940817 (Basic)
EP 610259 B1 970903
WO 9308523 930429
APPLICATION (CC, No, Date): EP 92921222 921012; WO 92EP2350 921012
PRIORITY (CC, No, Date): EP 91402797 911021
DESIGNATED STATES: DE; ES; FR; GB; IT
INTERNATIONAL PATENT CLASS: **G06F-007/50** ; **G06F-007/52**
NOTE:
  No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	940817 A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	940817 A1	Date of filing of request for examination: 940412
Change:	950607 A1	Representative (change)
*Assignee:	950607 A1	Applicant (transfer of rights) (change): THOMSON multimedia (1090174) 9, place des Vosges La Defense 5 F-92400 Courbevoie (FR) (applicant designated states: DE;ES;FR;GB;IT)
*Assignee:	950607 A1	Previous applicant in case of transfer of rights (change): THOMSON CONSUMER ELECTRONICS (S.A.) (1090171) 9, Place des Vosges La Defense 5 F-92400 Courbevoie (FR) (applicant designated states: DE;ES;FR;GB;IT)
Examination:	960131 A1	Date of despatch of first examination report: 951214
Change:	960807 A1	Representative (change)
Change:	970903 A1	Miscellaneous (change)
Grant:	970903 B1	Granted patent
*Assignee:	980325 B1	Proprietor of the patent (transfer of rights): THOMSON multimedia (1090172) 46, Quai A. Le Gallo 92648 Boulogne Cedex (FR) (applicant designated states: DE;ES;FR;GB;IT)
*Assignee:	980325 B1	Previous applicant in case of transfer of rights (change): THOMSON multimedia (1090174) 9, place des Vosges La Defense 5 92400 Courbevoie (FR) (applicant designated states: DE;ES;FR;GB;IT)
Oppn None:	980826 B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9708W5	588
CLAIMS B	(German)	9708W5	537
CLAIMS B	(French)	9708W5	583
SPEC B	(English)	9708W5	4156
Total word count - document A			0
Total word count - document B			5864
Total word count - documents A + B			5864

INTERNATIONAL PATENT CLASS: **G06F-007/50** ...
... **G06F-007/52**

...SPECIFICATION contains 4-bit full adders 611, 621, 616 and 626, 3-bit full adders 631 and 636 with normal carry input, a 3-bit full **adder** **635** with complementary carry input and 2:1 multiplexers 612 - 615, 622 - 625, 632 - 634, 617, 627 and 637. The input signals a0, b0, a1, b1, a2 and b3 of **adder** **635** stem from the **sum** and carry outputs of the basic building blocks FA in sixth row 418 which follow directly the respective adding circuit. The input signals of adders...represent output signals S20 - S23, S16 - S19 and S13 - S15 of the upper bits of the 24-bit result of the multiplication. Carry input of **adder** **635** is connected to the one clock delayed complementation command signal C' generated in Booth encoder circuit 408 which has been latched in static

latch 624. This latch is controlled by clock signals H and HB. The carry output of **adder 635** is connected to an inverter 641 and to the switching input of multiplexer 637. The output of inverter 641 is connected to the switching inputs...

...according to Fig. 12 the 3-bit adder has a complementary carry input CI.

E.g. the input signals a0 - a2 and b0 - b2 for **adder 635** are fed to respective connected parallel 1-bit adders. Input signals a0 and b0 and carry input CI are fed to adder 81 which outputs...

8/5,K/16 (Item 16 from file: 348)

00481389

Use of application programs on data in a heterogeneous data base system
Verwendung von Anwendungsprogrammen fur Daten in einem heterogenen Datenbanksystem
Utilisation de programmes d'application pour des donnees dans un systeme de base de donnees heterogene

PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (Proprietor designated states: all)
INVENTOR:
Adair, John Gary, 11519 Antigua Drive, Austin, Texas 78759, (US)
Demers, Richard Aime, 1318 21st Avenue, N.E., Rochester, Minnesota 55904, (US)
Ecimovic, Dusan, 4 Ramona Drive, Orinda, CA 94563, (US)
Jackson, Robert Dean, 2499 Schubert Avenue, San Jose, CA 95124, (US)
Lindsay, Bruce Gilbert, 1185 Settle Avenue, San Jose, CA 95125, (US)
Murphy, Michael Edward, 5203 Pickford Place, Durham, North Carolina 27703, (US)
Reinsch, Roger Alan, 20663 Greenleaf Drive, Cupertina, CA 95014, (US)
Resch, Robert Peter, Rte. 1, Bo 118, Byron, Minnesota 55920, (US)
Sanders, Richard Rolland, 1846 34th Street N.W., Rochester, Minnesota 55901, (US)
Selinger, Patricia Griffiths, 7215 Gold Creek Court, San Jose, 95120, (US)
Sunday, Robert Leo, 31 Willliam Street, Ontario L0G 1V0, (CA)
Zimowski, Melvin Richard, 1079 Surian Court, San Jose, CA 95120, (US)
LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)

PATENT (CC, No, Kind, Date): EP 449449 A2 911002 (Basic)
EP 449449 A3 930512
EP 449449 B1 020123
APPLICATION (CC, No, Date): EP 91302025 910311;
PRIORITY (CC, No, Date): US 500032 900327
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-017/30**

CITED REFERENCES (EP A):
HEWLETT-PACKARD JOURNAL vol. 37, no. 12, December 1986, PALO ALTO US pages 33 - 48 A. S. BROWN ET AL : 'Data BAse Management for HP Precision Architecture Computers'
INFORMATIONSTECHNIK IT vol. 29, no. 3, 1987, MUNCHEN BR pages 140 - 153 W. EFFELSBERG 'Datenbankzugriff in Rechnernetzen';
CITED REFERENCES (EP B):
HEWLETT-PACKARD JOURNAL vol. 37, no. 12, December 1986, PALO ALTO US pages 33 - 48 A. S. BROWN ET AL : 'Data BAse Management for HP Precision Architecture Computers'
INFORMATIONSTECHNIK IT vol. 29, no. 3, 1987, MUNCHEN BR pages 140 - 153 W. EFFELSBERG 'Datenbankzugriff in Rechnernetzen';

ABSTRACT EP 449449 A2
The present invention relates to a data base system comprising a first computer (10) which is used to execute an application program (14), a

data base (56) containing selected data for use in connection with the application program, a second computer (12) which is used to control the part of the data base system which contains the data base, the first and second computers being different types, means 17) for extracting from the application program data base commands which can be executed on the second computer but cannot be executed on the first computer, and means for replacing the extracted data base commands with call commands and for using the call commands to initiate the execution of the data base commands when required.

According to the invention the data base system is characterised in that it also comprises means (46, 50) for transmitting the data base commands to the second computer, and means (52) for utilising the call commands in the application program to initiate the execution of the data base commands by the second computer on the selected data in the data base. (see image in original document)

ABSTRACT WORD COUNT: 191

NOTE:

Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Change:	010425	A2	International Patent Classification changed: 20010306
Application:	911002	A2	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	030115	B1	No opposition filed: 20021024
Grant:	020123	B1	Granted patent
Examination:	920226	A2	Date of filing of request for examination: 911219
Search Report:	930512	A3	Separate publication of the European or International search report
Examination:	961120	A2	Date of despatch of first examination report: 961004

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	342
CLAIMS B	(English)	200204	698
CLAIMS B	(German)	200204	691
CLAIMS B	(French)	200204	890
SPEC A	(English)	EPABF1	14660
SPEC B	(English)	200204	14759
Total word count - document A			15004
Total word count - document B			17038
Total word count - documents A + B			32042

INTERNATIONAL PATENT CLASS: **G06F-017/30**

...SPECIFICATION name. Lines 625-632 process Output Host Variables in a manner similar to Host Variable processing in the replacement for Atomic database commands. Lines 633- **635 add** to the ModifiedProgramFile code in the language of the application program 14 to call the Database Interface Function for accessing a database item in the...

...SPECIFICATION name. Lines 625-632 process Output Host Variables in a manner similar to Host Variable processing in the replacement for Atomic database commands. Lines 633- **635 add** to the ModifiedProgramFile code in the language of the application program 14 to call the Database Interface Function for accessing a database item in the...

8/5,K/17 (Item 17 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00244336

A method and apparatus for contextual data enhancement.

Verfahren und Gerat fur kontextuale Datenverbesserung.

Methode et appareil pour ameliorer des donnees contextuelles.

PATENT ASSIGNEE:
Printrak International Incorporated, (823921), 1250 North Tustin Avenue, Anaheim, CA 92807, (US), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Capello, Richard D., 1911 Rushmore, Orange California 92667, (US)
Mabry, George R., 1250 Longview Drive, Fullerton California 92631, (US)
LEGAL REPRESENTATIVE:
Skone James, Robert Edmund et al (50281), GILL JENNINGS & EVERY Broadgate House 7 Eldon Street, London EC2M 7LH, (GB)
PATENT (CC, No, Kind, Date): EP 229028 A2 870715 (Basic)
EP 229028 A3 890809
EP 229028 B1 940316
APPLICATION (CC, No, Date): EP 87300063 870106;
PRIORITY (CC, No, Date): US 816865 860107
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-015/68**
CITED PATENTS (EP A): US 4398256 A

ABSTRACT EP 229028 A2

A method and apparatus for contextual data enhancement.

A fingerprint classification and identification method and apparatus including circuitry to analyze a fingerprint image in the form of an N x M matrix of data elements, such data being analyzed in three basic scan windows which are clocked through a matrix array of data elements each containing either intensity data, direction data or both. The first window and its associated circuitry (114,140,200,220) serve to estimate data element directions by analyzing the intensity data in selected direction slits in the window to establish the slit having the least summed contrast between data elements spaced apart in the slit by a selected number of data elements, or to establish that there does not clearly exist such a slit. The second window passes through the matrix such that its data elements have already been passed through the circuitry (114,140,200,220) associated with the preliminary direction estimate window and have a preliminary direction estimate of one of the slit directions or "no direction". This second window and its associated circuitry (114,230) enhance the direction estimates made during passage of the first window according to various logic tests which generally seek to identify a slit direction which, along with the directions adjacent to it, are the directions of the predominant number of data elements in the window, or which is the average of the two slit directions which comprise the largest and second largest number of data elements, if they are sufficiently close in direction. The final window examines data elements having enhanced directions and with its associated circuitry (240,210,114), enhances the intensity data of a center data element in the third window, provided the center data element has an enhanced direction other than "no direction", according to an analysis of the center data element and the neighboring slit data elements in the slit with the direction of the enhanced direction of the center data element. The center data element and the neighboring slit data elements are compared with each other for direction data and intensity data and are compared with a mean intensity value for the scan window to derive a correction value for the center data element intensity to arrive at an enhanced intensity value. Separate logic is used to enhance the center data element intensity when it has a direction of "no direction", after which the data is passed into classification and matching circuitry (161).

ABSTRACT WORD COUNT: 403

LEGAL STATUS (Type, Pub Date, Kind, Text):
Lapse: 020605 B1 Date of lapse of European Patent in a contracting state (Country, date): AT 19940316, BE 19940316, GR 19940316, IT 19940316, NL 19940316, SE 19940316,
Lapse: 20000126 B1 Date of lapse of European Patent in a contracting state (Country, date): AT 19940316, BE 19940316, GR 19940316, IT 19940316, NL 19940316,

Application:	870715 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	890809 A3	Separate publication of the European or International search report
Examination:	900411 A2	Date of filing of request for examination: 900208
Examination:	920102 A2	Date of despatch of first examination report: 911121
*Assignee:	931006 A2	Applicant (transfer of rights) (change): Printrak International Incorporated (823921) 1250 North Tustin Avenue Anaheim, CA 92807 (US) (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
Grant:	940316 B1	Granted patent
Lapse:	950111 B1	Date of lapse of the European patent in a Contracting State: AT 940316
Lapse:	950308 B1	Date of lapse of the European patent in a Contracting State: AT 940316, NL 940316
Oppn None:	950308 B1	No opposition filed
Lapse:	950315 B1	Date of lapse of the European patent in a Contracting State: AT 940316, BE 940316, NL 940316
Lapse:	991020 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19940316, BE 19940316, IT 19940316, NL 19940316,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	5352
CLAIMS B	(German)	EPBBF1	4925
CLAIMS B	(French)	EPBBF1	6379
SPEC B	(English)	EPBBF1	38835
Total word count - document A			0
Total word count - document B			55491
Total word count - documents A + B			55491

INTERNATIONAL PATENT CLASS: **G06F-015/68**

...SPECIFICATION one column in a delay circuit 634 and adding the output of the delay circuit 634 to the output of the circuit 631 in an **adder** **635** .

Referring to FIG. 22c, it can be seen that a lower group of eight magnitude subtractions may be obtained by first delaying the output of the **adder** **635** by two rows minus two columns in a delay circuit 636 and adding the output of the delay circuit 636 to the output of the **adder** **635** in an **adder** 637. Second, the output of the adder 637 is delayed four rows minus four columns in a delay 638 the output of which is added...

8/5,K/18 **(Item 18 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

00241947
Machine translation system
System zur maschinellen Ubersetzung
Systeme de traduction par machine
PATENT ASSIGNEE:
KABUSHIKI KAISHA TOSHIBA, (213130), 72, Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken 210, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Kumano, Akira, 102 Sugawarasunheights 6-3-1 Oofuna, Kamakura-shi Kanagawa-ken, (JP)
Sugawara, Yumiko, 5-606 Minamikandaijidanchi 2-9 Kandaiji, Kanagawa-ku Yokohama-shi Kanagawa-ken, (JP)
Aoyama, Chiaki, 3-7-2 Shirasagi Nakano-ku, Tokyo, (JP)

LEGAL REPRESENTATIVE:
Lehn, Werner, Dipl.-Ing. et al (7471), Hoffmann Eitle, Patent- und Rechtsanwalte, Postfach 81 04 20, 81904 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 247395 A2 871202 (Basic)
EP 247395 A3 880810
EP 247395 B1 940216
APPLICATION (CC, No, Date): EP 87106512 870506;
PRIORITY (CC, No, Date): JP 86113716 860520
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-017/28**
CITED REFERENCES (EP A):
FUJITSU-SCIENTIFIC & TECHNICAL JOURNAL, vol. 18, no. 1, March 1982, pages 117-133, Kawasaki, JP; S. SAWAI et al.: "Knowledge representation and machine translation"
PATENT ABSTRACTS OF JAPAN, vol. 6, no. 121 (P-126) 999 , 6th July 1982; & JP-A-57 48 161 (CANON K.K.) 19-03-1982;

ABSTRACT EP 247395 A2
To translate Japanese having no morphological distinction between singular and plural forms into English having a morphological distinction between the two, for instance, the dictionary unit (6) includes semantic information indicative of the plural number, and the translation unit (5) syntactically and semantically translates Japanese into English as follows: a Japanese sentence is morphologically analyzed into basic morphemes by an inflection information dictionary (6a); lexical syntactic information of the Japanese basic morphemes are retrieved from a word/phrase dictionary (6b); the Japanese sentence is syntactically analyzed into an intermediate structure by Japanese syntactic analysis grammar to clarify modification relationship between two words; the Japanese intermediate structure is semantically transferred into an English intermediate structure by structure transfer grammar; a concept data of a noun (e.g. "book") which includes FEATURE : NUMBER = PLURAL is formed when the noun is modified by an adjective (e.g. "many") indicative of the plural number; an English sentence structure is syntactically generated from the intermediate structure and by English syntactic generation grammar; and lastly an English morphemes are generated by morphological generation grammar to change "book" into "books".
ABSTRACT WORD COUNT: 186

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	871202	A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	880406	A2	Date of filing of request for examination: 880205
Search Report:	880810	A3	Separate publication of the European or International search report
Examination:	890510	A2	Date of despatch of first examination report: 890323
Grant:	940216	B1	Granted patent
Oppn:	950111	B1	Opposition 01/941115 Siemens Nixdorf Informationssysteme AG; Heinz-Nixdorf-Ring 1; D-33106 Paderborn; (DE) (Representative:)Fuchs, Franz-Josef, Dr.-Ing.; Postfach 22 13 17; D-80503 Munchen; (DE)
*Oppn:	980415	B1	Opposition (change) 01/941115 Siemens Nixdorf Informationssysteme AG; Heinz-Nixdorf-Ring 1; D-33106 Paderborn; (DE) (Representative:)Epping, Wilhelm, Dr.-Ing.; Patentanwalt Postfach 22 13 17; 80503 Munchen; (DE)
Amended:	981104	B2	Maintenance of the European patent as amended
Change:	981104	B1	International patent classification (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9845	449
CLAIMS B	(German)	9845	403
CLAIMS B	(French)	9845	567

SPEC B (English) 9845 3681
Total word count - document A 0
Total word count - document B 5100
Total word count - documents A + B 5100
INTERNATIONAL PATENT CLASS: **G06F-017/28**

...SPECIFICATION take proper account of plural forms where plurality is indicated only by a modifier.
An other example of a known machine translation system is disclosed **in** SPIE Vol. **635** Applications of Artificial Intelligence III (1986) p. 455 to 462 in the article entilted "A robust machine translation system" by R. Yoshii. Although described to...

8/5,K/32 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00484627
INTEGRATED BUSINESS SYSTEM FOR WEB BASED TELECOMMUNICATIONS MANAGEMENT
SYSTEME D'ECHANGES COMMERCIAUX INTEGRES POUR LA GESTION DE TELECOMMUNICATIONS SUR LE WEB
Patent Applicant/Assignee:
BARRY B Reilly,
CHODORONEK Mark A,
DeROSE Eric,
GONZALES Mark N,
JAMES Angela R,
LEVY Lynne,
TUSA Michael,
Inventor(s):
BARRY B Reilly,
CHODORONEK Mark A,
DeROSE Eric,
GONZALES Mark N,
JAMES Angela R,
LEVY Lynne,
TUSA Michael,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9915979 A1 19990401
Application: WO 98US20170 19980925 (PCT/WO US9820170)
Priority Application: US 9760655 19970926
Designated States: AU BR CA JP MX SG AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-013/00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 88075

English Abstract
The specification discloses a method of doing business over the public Internet, particularly, a method which enables access to legacy management tools used by a telecommunications enterprise in the management of the enterprise business to the enterprise customer, to enable the customer to more effectively manage the business conducted by the customer through the enterprise, this access being provided over the public Internet. This method of doing business is accomplished with one or more secure web servers which manage one or more secure client sessions over the Internet, each web server supporting secure communications with the client workstation; a web page backplane application capable of launching one or more management tool applications used by the enterprise. Each of the management tool applications provide a customer interface integrated within said web page which enables interactive Web/Internet based communications with the web servers; each web server supports communication of messages entered via the integrated customer interface to one or more remote enterprise management tool

application servers which interact with the enterprise management tool applications to provide associated management capabilities to the customer.

French Abstract

Cette invention se rapporte a un procede permettant de realiser des echanges commerciaux par l'Internet, en particulier un procede qui permet d'acceder a des outils de gestion legues utilises par une entreprise de telecommunications pour la gestion de ses relations commerciales avec ses clients, et pour permettre aux clients de gerer plus efficacement leurs interets commerciaux par l'intermediaire de l'entreprise, cet acces etant assure par l'Internet. Ce procede d'echanges commerciaux utilise un ou plusieurs serveurs web securises, qui gerent une ou plusieurs sessions client securisees sur l'Internet, chaque serveur web prenant en charge les communications securisees avec la station de travail client; ainsi qu'une application de fond de panier de page web capable de lancer une ou plusieurs applications d'outils de gestion utilisees par l'entreprise. Chacune de ces applications d'outils de gestion fournit une interface client integree a chaque page web qui permet des communications interactives par le Web/l'Internet avec les serveurs web; et chaque serveur web prend en charge la communication des messages entres via l'interface client integree a destination d'un ou de plusieurs serveurs d'applications d'outils de gestion d'entreprise distants, qui entrent en interaction avec les applications d'outils de gestion d'entreprise pour assurer aux clients des capacites de gestion associees.

Main International Patent Class: **G06F-013/00**
Fulltext Availability:
Detailed Description

Detailed Description
... be queried. It then
parses the metadata into a format which the COTS
software can readily convert into an SQL statement, as
indicated at step **635** , Figure 15(b), and **adds** the
report to the DSS report queue based upon type (Daily,
Weekly, Monthly, Adhoc) and associated DataMart, as
indicated at step 638. It should be...

8/5,K/34 (Item 16 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00483321
DATA TRANSFER TO A NON-VOLATILE STORAGE MEDIUM
TRANSFERT DE DONNEES VERS UNE MEMOIRE REMANENTE
Patent Applicant/Assignee:
PHOENIX TECHNOLOGIES LTD,
LEWIS Timothy,
Inventor(s):
LEWIS Timothy,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9914673 A1 19990325
Application: WO 98US19128 19980916 (PCT/WO US9819128)
Priority Application: US 97931330 19970916
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-011/14**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 11302

English Abstract

To improve the speed of transition to the zero-volt suspend state, system context is saved from volatile random access memory to non-volatile memory, such as a hard disk, using a compression algorithm which speeds the transfer of data to non-volatile memory by recognizing data pages having bytes of a single value. The system context in extended memory of RAM consists of a number of system context memory blocks, and between these memory blocks are memory holes containing information which does not require storage. Initially, the entirety of data in a buffer region of RAM is stored directly to disk. Then, successive pages from each system context memory block are transferred to the buffer, where the page size corresponds to the memory management unit page size. When testing locates a region of heterogeneous entries, then a heterogeneous data flag, the length of the heterogeneous region, and the heterogeneous data region are transferred to the buffer. When testing determines that a page contains bytes of a single value, then a compression flag representing that value is substituted for that page. When a memory hole is reached, a memory hole flag and the size of the memory hole are transferred to the buffer. On each transfer of a byte of data to the buffer it is determined whether the buffer is full, and when it is full then a write-to-disk is performed. To transition from the zero-volt suspend state back to an operational state, bytes are transferred from the hard disk to the buffer whenever all the bytes currently in the buffer have been transferred to extended memory. When testing of the buffer entries locates a heterogeneous data flag, the value immediately following the flag is determined, and a data region having a length of that value is transferred to extended memory. When a compression flag is found, a 4 kilobyte page of the corresponding byte value is transferred to extended memory. When a memory hole flag is found, a memory hole with a length of the value immediately following the memory hole flag is created in extended memory.

French Abstract

Pour accroitre la vitesse de transition vers l'etat de suspension a zero volt, le contexte d'un systeme est sauvegarde d'une memoire vive non remanente vers une memoire remanente, tel un disque dur, au moyen d'un algorithme de compression qui permet d'activer le transfert de donnees vers la memoire remanente par une reconnaissance de pages de donnees comportant des octets d'une seule valeur. Le contexte du systeme situe dans une memoire etendue de la RAM consiste en un certain nombre de blocs de memoire de contexte systeme, entre lesquels se trouvent des trous de memoire contenant des informations ne necessitant pas de stockage. Initialement, l'integrite des donnees d'une zone tampon de la RAM est stockee directement sur le disque. Puis des pages successives de chaque bloc de memoire de contexte systeme sont transferees vers le tampon, a l'endroit ou la taille de page correspond a la taille de page de l'unite de gestion de memoire. Lorsqu'un essai permet de localiser une zone d'entrees heterogenes, un indicateur de donnees heterogenes, la longueur de la zone heterogene et la zone de donnees heterogenes sont transferes vers le tampon. Lorsqu'un essai permet de determiner qu'une page contient des octets d'une seule valeur, un indicateur de compression representant cette valeur est substitue a cette page. Lorsqu'un trou de memoire est atteint, un indicateur de trou de memoire et la taille du trou de memoire sont transferes vers le tampon. Lors de chaque transfert d'un octet de donnees vers le tampon, on determine si le tampon est plein, et le cas echeant, une inscription est effectuee sur le disque. Pour effectuer la transition entre l'etat de suspension a zero volt et un etat operationnel, des octets sont transferes du disque dur vers le tampon lorsque tous les octets presents dans le tampon ont ete transferes vers la memoire etendue. Lorsqu'un essai des entrees de tampon permet de localiser un indicateur de donnees heterogenes, la valeur qui suit immediatement l'indicateur est determinee, et une zone de donnees presentant une longueur de cette valeur est transferee vers la memoire etendue. Lorsqu'un indicateur de compression est trouve, une page de 4 kilo-octets de la valeur d'octet correspondante est transferee vers la memoire etendue. Lorsqu'un indicateur de trou de memoire est trouve, un trou de memoire presentant une longueur de la valeur qui suit

immediatement l'indicateur de trou de memoire est produit dans la memoire etendue.

Main International Patent Class: **G06F-011/14**
Fulltext Availability:
Detailed Description

Detailed Description
... transfer size must be performed by pniDiskWrite, so Sectors is set equal 630 to Size/SectorSize before a write to disk is performed by pmDiskWrite **635** . Then 640, (Sectors*SectorSize) is **subtracted** from Size so
14
that Size represents the quantity of data which remains in the buffer 120 to be written to disk, and Location i...

8/5,K/35 (Item 17 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00444826 **Image available**
SYSTEM AND METHOD FOR A FAST CARRY/SUM SELECT ADDER
SYSTEME ET PROCEDE POUR SOMMATEUR SELECTIONNEUR RAPIDE DE REPORT/SOMME
Patent Applicant/Assignee:
S3 INCORPORATED,
Inventor(s):
RANJAN Nalini,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9835290 A1 19980813
Application: WO 98US936 19980120 (PCT/WO US9800936)
Priority Application: US 97788391 19970127
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-007/50**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 14342

English Abstract
An adder system (100) includes at least one adder block subsystem (102a). Each adder block subsystem includes a pair of input signal lines (130a-h and 133a-h), an adder circuit block having a conditional sum-select and a conditional carry-select (110), a sum-high line (220a-h), a sum-low line (225a-h), a carry-high line (260h), carry-low line (265h), a sum selection switch (160), a carry selection switch (163), a carry forward line (199a), and an output signal line (185). The input lines are individual bit lines that are paired together from the least significant bit to the most significant bit. Within the adder circuit block, pairs of the input bit lines are coupled to the conditional sum-select and the conditional carry-select. The conditional sum-select is coupled to the sum-high and sum-low lines and the conditional carry-select is coupled to the carry-high and carry-low line. The sum selection switch selectively couples the output signal line to the sum-high or the sum-low line.

French Abstract
Systeme sommateur (100) comprenant au moins un sous-systeme de bloc sommateur (102a). Chacun de ces sous-systemes comporte une paire de lignes de signaux d'entree (13a-h et 133a-h). Un bloc de circuits sommateurs a les elements suivants : selection de somme conditionnelle et selection de report conditionnel (110), ligne de somme haute (220a-h) ,

ligne de somme basse (225a-h), ligne de report haut (260h), ligne de report bas (265h), commutateur de selection de somme (160), commutateur de selection de report (163), ligne de report en avant (199a), et ligne de signaux de sortie (185). Les lignes d'entree sont des lignes binaires individuelles appariees, du bit de poids faible au bit de poids fort. Dans le bloc de circuits sommateurs, les paires de lignes binaires d'entree sont couplees a la selection de somme conditionnelle et a la selection de report conditionnel. Cette derniere est couplee a la ligne de report haut et a la ligne de report bas. Le commutateur de selection de somme assure le couplage selectif entre la ligne de report haut ou la ligne de report bas et la ligne de report en avant.

Main International Patent Class: **G06F-007/50**
Fulltext Availability:
Detailed Description

Detailed Description
... line 199a. If the carry signal along the carry forward line 199a is a logic high, the sum output selection switch 166 of the second **adder** block subsystem 102b selects **635** the **sum** -high line 230 that is coupled to the second adder circuit block 115. If the carry signal along the carry forward line 199a is a...

...low line 285h, 295h.

The 8-bit output signal along the third output signal line 191 of the third adder subsystem 102c is either the **sum** signal selected **635** along the **sum** -high line 240 if the carry signal along the carry forward line 199b of the second adder block subsystem 102b is a logic high, or is the **sum** signal selected **635** along the **sum** -low ...a logic low.

The 8-bit output signal along the fourth output signal line 194 of the fourth adder block subsystem 102d is either the **sum** signal selected **635** along the **sum** -high line 250 if the carry signal along the carry forward line 199c of the third adder block subsystem 102c is a logic high, or is the **sum** signal selected **635** along the **sum** -low line 255 if the carry signal along the carry forward line 199c of the third adder block subsystem 102c is a logic low. The...

8/5,K/36 (Item 18 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00343192
HIGH ACCURACY, AUTOMATICALLY CONTROLLED VARIABLE LINEAR SEED SPACING PLANTING APPARATUS
SEMOIR HAUTE PRECISION, A COMMANDE AUTOMATIQUE, AVEC ESPACEMENT LINEAIRE VARIABLE DES SEMAILLES
Patent Applicant/Assignee:
FLUID POWER INDUSTRIES INC,
Inventor(s):
HARMS Louis C,
ROSENBROCK Richard,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9625704 A1 19960822
Application: WO 96US1880 19960208 (PCT/WO US9601880)
Priority Application: US 95388214 19950213
Designated States: AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LT LU LV MD MG MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TT UA UG UZ VN KE LS MW SD SZ UG AZ BY KG KZ RU TJ TM AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-007/00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims

Fulltext Word Count: 31993

English Abstract
A control system for a mobile planting apparatus (24) which permits discrete plant spacing to be determined and maintained independent of any wheel (6) rotation on the planting apparatus (24) or towing apparatus (8) is disclosed, having: (1) a ground speed sensor (26) wherein the rate of movement relative to the ground is determined independent of the wheel (6) rotation of the planting apparatus (24) or towing apparatus (8); (2) an input/display device (62) for inputting desired linear plant spacing; (3) a variable speed motor (42) for mechanically driving seed metering devices (12) on the planting apparatus (24) at varying rates independent of any wheel (6) rotation of the planting apparatus (24) or towing apparatus (8), wherein the motor (42) changes speeds in response to an electronic signal; (4) a programmable control circuit (60) communicating electronically with the input/display device (62) and ground speed sensor (26).

French Abstract
On decrit un systeme de commande destine a un semoir (24) mobile et permettant de determiner un espacement distinct des vegetaux et de conserver cet espacement en le rendant independant de toute rotation des roues (6) du semoir (24) ou de l'element tractant (8), ce systeme comprenant: (1) un capteur (26) de vitesse au sol dans lequel la vitesse de deplacement par rapport au sol est determinee independamment de la rotation des roues (6) du semoir (24) ou de l'element tractant (8); (2) un dispositif (62) d'entree/affichage destine a l'entree de l'espacement lineaire souhaite des vegetaux; (3) un moteur (42) a vitesse variable servant a entrainer mecaniquement des dispositifs (12) doseurs de semailles situes sur le semoir (24), a des vitesses variables, independantes de toute rotation (6) des roues du semoir (24) ou de l'element tractant (8), ce moteur (42) changeant de vitesse en reponse a un signal electronique; (4) un circuit (60) de commande programmable communiquant de facon electronique avec le dispositif (62) d'entree/affichage et le capteur (26) de vitesse au sol.

Main International Patent Class: **G06F-007/00**
Fulltext Availability:
Detailed Description

Detailed Description
... D TCX4
0 6 3 2!380 di SC 5 XEND
'@633 !282 dd :c
4 TOC4
C634 fJ84 dc 66 4 LOD SPEZD@2
: **635** !386 cJ :C 40 4 **ADDO** OS0040
:636 !389 dd. 66 4 SM SPEED*2
f38b 96 6 5 3 LZAA SPEED+!
0638 f 38d 89 3C 2 ADCA #Soo
:639...

8/5,K/37 (Item 19 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00262476 **Image available**
A DYNAMIC GRAPHICAL SYSTEM CONFIGURATION UTILITY
PROGRAMME UTILITAIRE DE CONFIGURATION DE SYSTEME GRAPHIQUE DYNAMIQUE
Patent Applicant/Assignee:
INTELLUTION INC,
Inventor(s):
RUBIN Stephen E,
VANSLETTE Paul J,
FAVREAU Scott,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9410645 A1 19940511

Application: WO 93US10278 19931027 (PCT/WO US9310278)
Priority Application: US 92968061 19921028
Designated States: AU BR CA JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-015/62**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 12228

English Abstract
The invention provides a graphics-oriented technique for enabling a user to configure data processing features of a computer system (10) that includes at least one computer. The data processing features are presented to the user in the form of displayed graphical objects (52-58), each of which represents one feature. The user selects a graphical object (52-58) using an input device of the computer (e.g., a mouse (122a, 120c)), and is then prompted to enter information associated with the data processing feature represented by the selected object (52-58). Thereafter, the computer system (10) is enabled to use the data processing feature to process data in accordance with the user-specified information. After the configuration information has been entered for at least some of the objects (52-58), symbols are added to the display (120a, 120b) to indicate that the data processing features that the objects (52-58) represent have been enabled, thereby presenting to the user a comprehensive, easily understood representation of the current configuration state of the system (10).

French Abstract
L'invention se rapporte a une technique graphique permettant a un utilisateur de configurer des caracteristiques de traitement de donnees d'un systeme informatique (10) qui comprend au moins un ordinateur. Les caracteristiques de traitement de donnees sont presentees a l'utilisateur sous forme d'objets graphiques affiches (50) dont chacun represente une caracteristique. L'utilisateur selectionne un objet graphique (52-58) a l'aide d'un dispositif d'entree de l'ordinateur (par exemple une souris (122a, 120c)), puis est guide afin d'introduire des informations associees a la caracteristique de traitement de donnees representee par l'objet selectionne (52-58). A partir de ce moment, le systeme informatique (10) peut utiliser la caracteristique de traitement de donnees pour traiter des donnees en fonction des informations specifiees par l'utilisateur. Apres que les informations de configuration ont ete introduites pour au moins quelques-uns des objets (52-58), des symboles sont ajoutes a l'affichage (120a, 120b) afin d'indiquer que les caracteristiques de traitement de donnees que representent les objets (52-58) ont ete validees, ce qui fournit a l'utilisateur une representation globale et facile a comprendre de l'etat de configuration actuel du systeme (10).

Main International Patent Class: **G06F-015/62**
Fulltext Availability:
Detailed Description
Detailed Description
... is using to configure system 10),
The user then selects an appropriate driver from list and then selects the "OK" button, The user then selects " **Add** " button **635** . SCU program 124 **adds** the I/O driver to the list of configured I/O drivers shown in list 628. if the user wishes to remove an I/O...

8/5,K/38 (Item 20 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00252667 **Image available**
BEARING DESIGN ANALYSIS APPARATUS AND METHOD

APPAREIL ET PROCEDE DE CONCEPTION D'ANALYSE DE PALIERS
Patent Applicant/Assignee:
KMC INC,
IDE Russell D,
Inventor(s):
IDE Russell D,
PAQUETTE Donald J,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9400819 A1 19940106
Application: WO 93US5799 19930621 (PCT/WO US9305799)
Priority Application: US 92811 19920623
Designated States: AU BR CA JP KR NO AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-015/20**
International Patent Class: **G06F-15:60**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 39616

English Abstract
A method and apparatus for designing hydrodynamic bearings having movable bearing pads and a method for supporting a rotating shaft with such bearings. Bearing pad position under load is calculated using finite element analysis to determine influence coefficients, which are then used in conjunction with a two-dimensional model of the fluid film to provide the steady-state behavior of the bearing. The bearing design is altered until an acceptable design is arrived at. A bearing designed according to this method can be used to support a rotating shaft.

French Abstract
L'invention se rapporte a un procede et a un appareil permettant de concevoir des paliers hydrodynamiques a patins mobiles et a un procede visant a supporter un arbre rotatif avec ces paliers. La position du patin de palier sous la charge est calculee par analyse d'elements finis afin de determiner les coefficients d'influence qui sont ensuite utilises conjointement avec un modele bidimensionnel du film d'huile pour obtenir la tenue stable du palier. Ce type de palier est modifie jusqu'a obtention d'une conception acceptable. Un palier concu selon ce procede peut etre utilise pour supporter un arbre rotatif.
Main International Patent Class: **G06F-015/20**
International Patent Class: **G06F-15:60**
Fulltext Availability:
Detailed Description

Detailed Description
... outer beam 544 into three
beams,
- 73
The support structure for bearing pad 525 is
similar to that for bearing pad 522 except that an **addi**
tional opening **635** non-symmetrically divides the outer
beam 544 into two beams, By virtue of the non-symmetri
cal division of the outer beam 544, the bearing...

8/5,K/39 (Item 21 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00234264 **Image available**
1-BIT ADDER AND MULTIPLIER CONTAINING A 1-BIT ADDER
ADDITIONNEUR 1 BIT ET MULTIPLICATEUR LE COMPORTANT
Patent Applicant/Assignee:
THOMSON CONSUMER ELECTRONICS S A,
CHAN YAN FONG Joseph,
Inventor(s):

CHAN YAN FONG Joseph,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9308523 A2 19930429
Application: WO 92EP2350 19921012 (PCT/WO EP9202350)
Priority Application: FR 91402797 19911021
Designated States: JP KR US AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
Main International Patent Class: **G06F-007/50**
International Patent Class: **G06F-07:52**
Publication Language: French
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 6127
English Abstract

E.g. for video applications fast multipliers with high resolution are required. But a higher resolution results in more partial products to be calculated internally. The Booth-Mc Sorley algorithm can be used in order to reduce the required number of such partial products. This algorithm can be combined with a diagonal propagation of the carry from one partial product to the other, allowing all the sums on a line to be calculated simultaneously. But the reachable multiplication time is not short enough. The inventive multiplier in nearly full CMOS design has been constructed with a 1.2 mu BICMOS technology, having a multiplication time of 9 ns with a supply voltage of 5 volts. Minimum multiplication time has been achieved by a combination of the following techniques: use of the Booth-Mc Sorley algorithm in order to reduce the number of partial products; diagonal propagation of the carry from one partial product to the other allowing all the sums on one line to be done simultaneously; use of the carry select approach in the final 14 bits adder and in the first two adders in the intermediate rows; use of inventive fast one-bit full adders with complementary pass transistor logic.

French Abstract

Les applications dans le domaine de la video, par exemple, necessitent des multiplicateurs rapides a haute definition, mais une definition plus elevee entraine un accroissement du nombre de produits partiels a calculer de maniere interne. On peut utiliser l'algorithme de Booth-McSorley afin de reduire le nombre requis de ces produits partiels. Cet algorithme peut s'associer a une propagation diagonale du report entre l'un des produits partiels et un autre, ce qui permet un calcul simultane de l'ensemble des sommes d'une meme ligne. Malgre cela, le temps de multiplication ainsi obtenu n'est toujours pas suffisamment court. On a prevu un multiplicateur de conception presque entierement CMOS construit a l'aide d'une technologie BICMOS a 1,2 mum, son temps de multiplication etant de 9 ns lorsque la tension d'alimentation est de 5 volts. On a minimise le temps de multiplication en combinant entre elles les techniques suivantes: l'utilisation de l'algorithme de Booth-McSorley afin de reduire le nombre de produits partiels; la propagation diagonale du report entre l'un des produits partiels et un autre, ce qui permet le calcul simultane de l'ensemble des sommes d'une meme ligne; l'utilisation de l'approche de selection de report dans le dernier additionneur 14 bits et dans les deux premiers additionneurs des rangees intermediaires; et l'utilisation de ces additionneurs 1 bit complets et rapides a logique a transistors ballast complementaires.

Main International Patent Class: **G06F-007/50**
International Patent Class: **G06F-07:52**
Fulltext Availability:
Detailed Description
Claims

Detailed Description
... 4-bit full ad
ders 611, 621, 616 and 626, 3-bit full adders 631 and 636 with normal carry input, a 3-bit full **adder** **635** with complementary carry input and 2:1 multiplexers 612 - 615, 622 625,e 632 - 634r 617, 627 and 637. The- input signals aO, bO, ai, bl, a2 and b3 of **adder** **635** stem from the **sum** and carry

outputs of the basic building blocks FA in sixth row 418
which follow directly the respective adding circuit. The in-
put signals of...

...represent output signals S20
S23, S16 - S19 and S13 - S15 of the upper bits of the 24-bit
result of the multiplication. Carry input of **adder 635** is
connected to the one clock delayed complementation command
signal C' generated in Booth encoder circuit 408 which has
been latched in static latch 624. This latch is controlled
by clock signals H and HB. The carry output of **adder 635** is
connected to an inverter 641 and to the switching input of
multiplexer 637. The output of ...cording to Fig. 12 the 3-bit adder has
a complementary carry
nput CI.

E.g. the input signais aO - a2 and bO.- b2 for **adder 635** are
fed to respective connected parallel 1-bit adders. Input sig
nais aO and bO and carry input CI are fed to adder 81 which...

Claim
... pipeline row (413, 416e
419);
- a last row (410) with a carry select adder circuit
which is constructed from one 4- and/or 3-bit **adder** cir
cuit (**635**) and/or pairs of said 4- and/or 3-bit adder
circuits (611,616; 621,626; 631,636). which contain
said 1-bit adders

4...

8/5,K/40 (Item 22 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00126982
FAULT DETECTION ARRANGEMENT FOR A DIGITAL CONFERENCING SYSTEM
DISPOSITIF DE DETECTION DE FAUTES POUR UN SYSTEME NUMERIQUE DE CONFERENCE
Patent Applicant/Assignee:
AMERICAN TELEPHONE & TELEGRAPH COMPANY,
Inventor(s):
BARANYAI Lawrence,
COLTON John Robert,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8505238 A1 19851121
Application: WO 85US603 19850405 (PCT/WO US8500603)
Priority Application: US 84829 19840507
Designated States: AT BE CH DE FR GB IT JP KR LU NL SE
Main International Patent Class: H04M-003/56
International Patent Class: **G06F-11:10**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 14121
English Abstract
Error/fault detection in signal processing systems such as those
employed in a time division multiplex conferencer. The digital message
samples (of the conferees) and the accompanying parity bits are delivered
to a signal processor e.g., a binary arithmetic adder (10). The adder
sums the message samples and this sum is coupled to a first parity tree
(11), which in response thereto generates a first parity bit. The carries
generated by the summing operation are coupled to a second parity tree
(12) along with the message parity bits and the second parity tree
generates a second parity bit therefrom. The first and second parity bits
are compared (13) and if they differ a fault exists. Corrective action is
taken immediately--the faulty conference "leg" is removed from the

conference connection without affecting the remaining legs in the conference or any other conference.

French Abstract

Detecteur d'erreur/panne dans un systeme de traitement de signaux tels que ceux employes dans un systeme de conference multiplex par partage de temps. Les echantillons de messages numeriques (des conferences) et les bits de parite qui les accompagnent sont livres a une machine de traitement de signaux, par exemple, a un additionneur numerique binaire (10). L'additionneur additionne les echantillons de messages et cette somme est couplee a un premier arbre de parite (11), qui y repond en produisant un premier bit de parite. Les reports produits par l'operation d'addition sont couples a un deuxieme arbre de parite (12) avec les bits de parite du message, et le deuxieme arbre de parite produit a partir de ceux-ci un deuxieme bit de parite. Le premier et le deuxieme bits de parite sont compares (13) et, s'ils sont differents, il existe une panne. Des mesures correctives sont prises immediatement - la "branche" defectueuse de la conference est enlevee de la connexion de la conference sans affecter les branches restantes dans cette conference ou dans toute autre conference.

International Patent Class: **G06F-11:10**
Fulltext Availability:
Detailed Description

Detailed Description

... message
sample previously stored in sample RAM 610, it is essentially subtracted by out-adder 640 from the summed - 39
message sample inputted via bus **635** by the twos-complement **addition** . A message sample respective to a time slot is effectively subtracted in this manner from the summed message sample to eliminate its message contribution from...

...output select circuit 710
via leads POOR or NOOR in the event either positive or negative overflow occurs as a result of summing an inputted **summed** message sample from bus **635** with a respective message sample inputted from bus 626.